

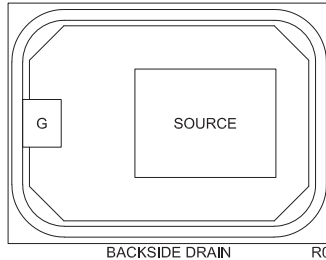
CP390-CDM4-600LR

N-Channel MOSFET Die

Enhancement-Mode

The CP390-CDM4-600LR is a silicon N-Channel MOSFET designed for high current applications.

MECHANICAL SPECIFICATIONS:



Die Size	117 x 87.4 MILS
Die Thickness	9.1 MILS
Gate Bonding Pad Size	14 x 17.3 MILS
Source Bonding Pad Size	51.2 x 39.4 MILS
Top Side Metalization	Al – 43,000Å
Back Side Metalization	Ag – 8,000Å
Scribe Alley Width	3.15 MILS
Wafer Diameter	6 INCHES
Gross Die Per Wafer	2,154

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	30	V
Continuous Drain Current (Steady State)	I_D	4.0	A
Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$	I_{DM}	13.5	A
Continuous Source Current (Body Diode)	I_S	4.0	A
Maximum Pulsed Source Current (Body Diode)	I_{SM}	13.5	A
Single Pulse Avalanche Energy (Note 1)	E_{AS}	197	mJ
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Note 1: $L=30\text{mH}$, $I_{AS}=3.5\text{A}$, $V_{DD}=100\text{V}$, $R_G=25\Omega$, Initial $T_J=25^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)						
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
I_{GSSF}, I_{GSSR}	$V_{GS}=30\text{V}, V_{DS}=0$			100	nA	
I_{DSS}	$V_{DS}=600\text{V}, V_{GS}=0$		0.065	1.0	μA	
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	600			V	
$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	2.0	3.25	4.0	V	
V_{SD}	$V_{GS}=0, I_S=4.0\text{A}$		0.86	1.4	V	
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=2.0\text{A}$		0.65	0.95	Ω	
C_{rss}	$V_{DS}=100\text{V}, V_{GS}=0, f=1.0\text{MHz}$		1.31		pF	
C_{iss}	$V_{DS}=100\text{V}, V_{GS}=0, f=1.0\text{MHz}$		328		pF	
C_{oss}	$V_{DS}=100\text{V}, V_{GS}=0, f=1.0\text{MHz}$		26		pF	
$Q_{g(tot)}$	$V_{DS}=480\text{V}, V_{GS}=10\text{V}, I_D=4.0\text{A}$ (Note 2)		11.59		nC	
Q_{gs}	$V_{DS}=480\text{V}, V_{GS}=10\text{V}, I_D=4.0\text{A}$ (Note 2)		2.04		nC	
Q_{gd}	$V_{DS}=480\text{V}, V_{GS}=10\text{V}, I_D=4.0\text{A}$ (Note 2)		6.09		nC	

CP390-CDM4-600LR

Typical Electrical Characteristics

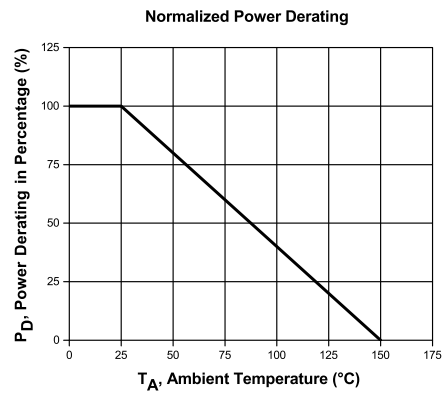
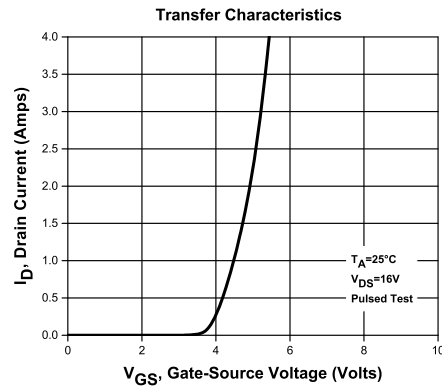
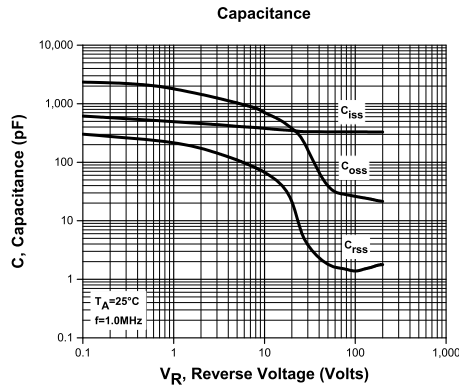
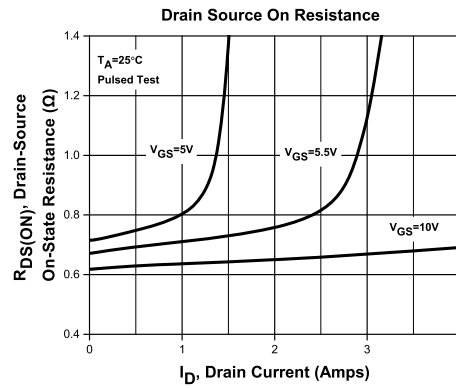
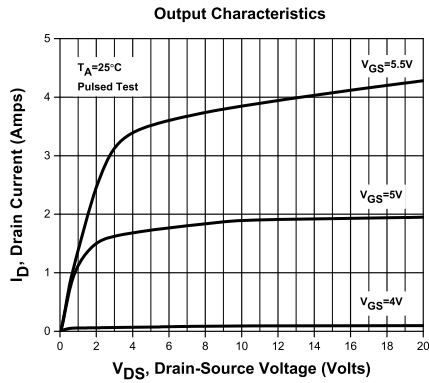
ELECTRICAL CHARACTERISTICS - Continued: ($T_A=25^{\circ}\text{C}$)

SYMBOL	TEST CONDITIONS	TYP	UNITS
$t_{d(on)}$	$V_{DD}=300\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	8.0	ns
t_r	$V_{DD}=300\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	24	ns
$t_{d(off)}$	$V_{DD}=300\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	33	ns
t_f	$V_{DD}=300\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	24	ns
t_{rr}	$V_{GS}=0$, $I_S=4.0\text{A}$, $di/dt=100\text{A}/\mu\text{s}$ (Note 2)	211	ns
Q_{rr}	$V_{GS}=0$, $I_S=4.0\text{A}$, $di/dt=100\text{A}/\mu\text{s}$ (Note 2)	1.7	μC

Note 2: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

CP390-CDM4-600LR

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

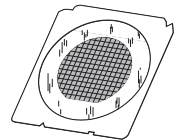
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

Worldwide Distributors:
www.centrasemi.com/wwdistributors

For the latest version of Central Semiconductor's **LIMITATIONS AND DAMAGES DISCLAIMER**, which is part of Central's Standard Terms and Conditions of sale, visit: www.centrasemi.com/terms