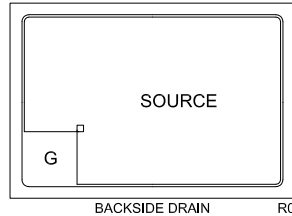


CP398X-CTLDM303N

N-Channel MOSFET Die

Enhancement-Mode

The CP398X-CTLDM303N is a silicon N-Channel MOSFET designed for high speed pulsed amplifier and driver applications.



MECHANICAL SPECIFICATIONS:

Die Size	37.8 x 26 MILS
Die Thickness	5.5 MILS
Gate Bonding Pad Size	7.3 x 7.3 MILS
Source Bonding Pad Size	34 x 22.2 MILS
Top Side Metalization	Al – 40,000Å
Back Side Metalization	Ti/Ni/Ag – 1,000Å/3,000Å/10,000Å
Scribe Alley Width	2.36 MILS
Wafer Diameter	8 INCHES
Gross Die Per Wafer	45,000

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

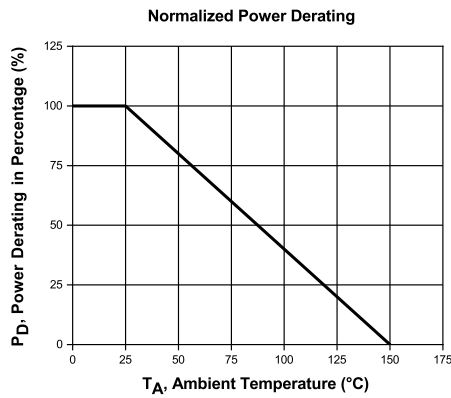
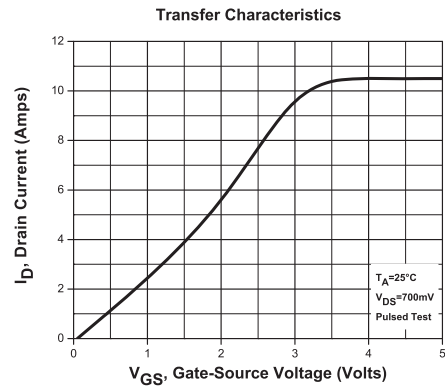
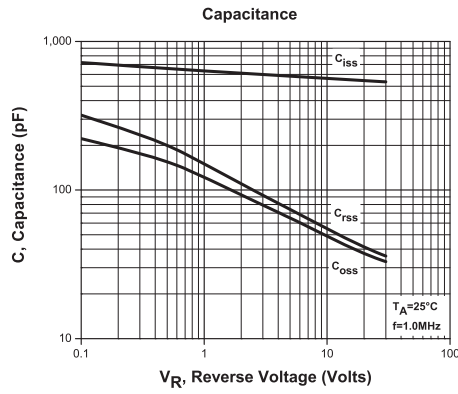
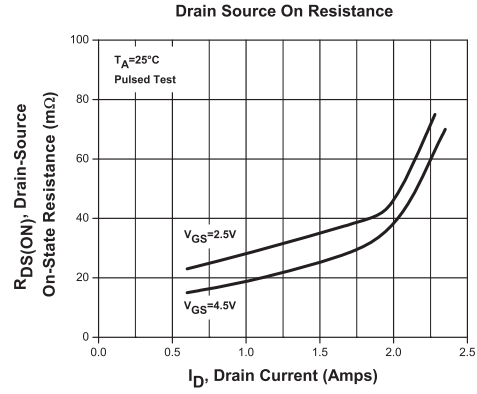
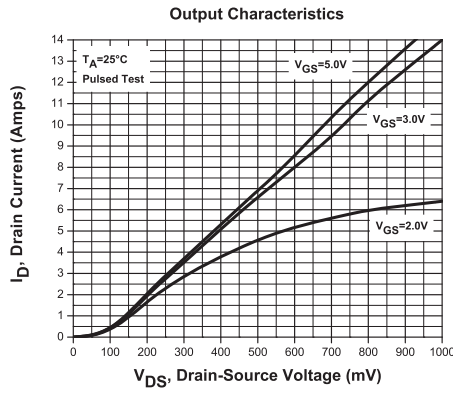
	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	12	V
Continuous Drain Current (Steady State)	I_D	3.6	A
Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$	I_{DM}	14.4	A
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=12\text{V}, V_{DS}=0$			10	μA
I_{DSS}	$V_{DS}=20\text{V}, V_{GS}=0$			1.0	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	30			V
$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	0.6		1.2	V
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=1.8\text{A}$			0.04	Ω
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=1.8\text{A}$			0.078	Ω
$Q_{g(tot)}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=3.6\text{A}$			13	nC
Q_{gs}	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=3.6\text{A}$			1.4	nC
Q_{gd}	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=3.6\text{A}$			2.7	nC
g_{FS}	$V_{DS}=5.0\text{V}, I_D=3.6\text{A}$		11.8		S
C_{rss}	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		55		pF
C_{iss}	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		590		pF
C_{oss}	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		50		pF
t_{on}	$V_{DD}=10\text{V}, V_{GS}=4.0\text{V}, I_D=3.6\text{A}, R_G=10\Omega$		15		ns
t_{off}	$V_{DD}=10\text{V}, V_{GS}=4.0\text{V}, I_D=3.6\text{A}, R_G=10\Omega$		29		ns

CP398X-CTLDM303N

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

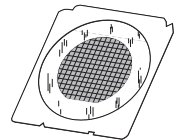
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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