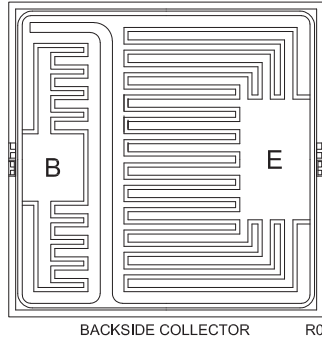


CP527-2N6042

PNP - Darlington Transistor Die

8.0 Amp, 100 Volt

The CP527-2N6042 is a silicon PNP Darlington power transistor designed for high gain amplifier applications.



MECHANICAL SPECIFICATIONS:

Die Size	110 x 110 MILS
Die Thickness	10.6 MILS
Base Bonding Pad Size	21 x 24 MILS
Emitter Bonding Pad Size	24 x 42 MILS
Top Side Metalization	Al – 20,000Å
Back Side Metalization	Ni/Ag – 2,000Å/10,000Å
Scribe Alley Width	4.3 mils
Wafer Diameter	4 INCHES
Gross Die Per Wafer	875

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	100	V
Collector-Emitter Voltage	V_{CEO}	100	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	8.0	A
Peak Collector Current	I_{CM}	16	A
Continuous Base Current	I_B	120	mA
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

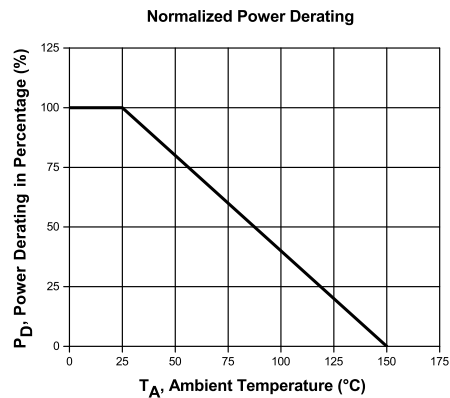
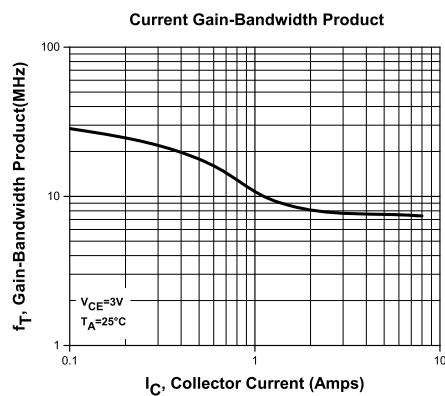
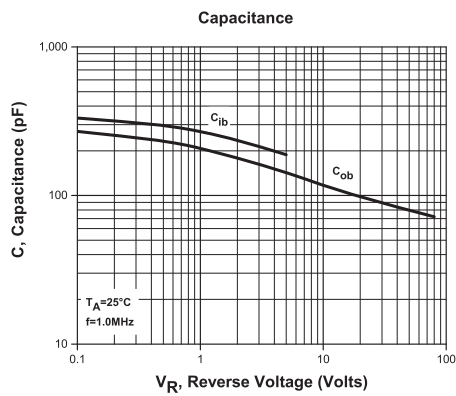
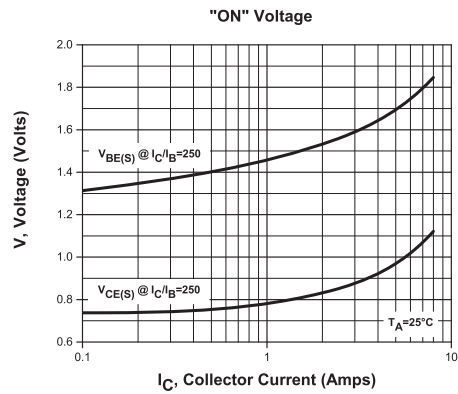
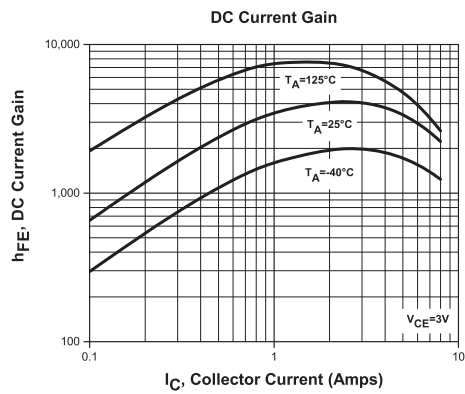
ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=100\text{V}$		20	μA
I_{CEV}	$V_{CE}=100\text{V}, V_{BE(OFF)}=1.5\text{V}$		20	μA
I_{CEO}	$V_{CE}=100\text{V}$		20	μA
I_{EBO}	$V_{EB}=5.0\text{V}$		2.0	mA
BV_{CEO}	$I_C=100\text{mA}$	100		V
$V_{CE(SAT)}$	$I_C=3.0\text{A}, I_B=12\text{mA}$		2.0	V
$V_{CE(SAT)}$	$I_C=8.0\text{A}, I_B=80\text{mA}$		4.0	V
$V_{BE(SAT)}$	$I_C=8.0\text{A}, I_B=80\text{mA}$		4.5	V
$V_{BE(ON)}$	$V_{CE}=4.0\text{V}, I_C=4.0\text{A}$		2.8	V
h_{FE}	$V_{CE}=4.0\text{V}, I_C=3.0\text{A}$	1.0K	20K	
h_{FE}	$V_{CE}=4.0\text{V}, I_C=8.0\text{A}$	100		
h_{fe}	$V_{CE}=4.0\text{V}, I_C=3.0\text{A}, f=1.0\text{kHz}$	300		
f_T	$V_{CE}=4.0\text{V}, I_C=3.0\text{A}, f=1.0\text{MHz}$	4.0		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=100\text{kHz}$		300	pF

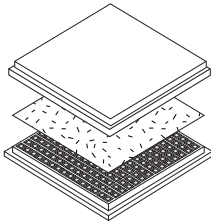
R0 (28-June 2016)

CP527-2N6042

Typical Electrical Characteristics



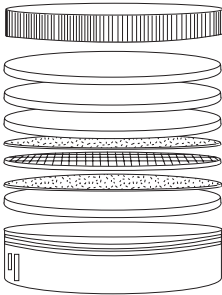
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

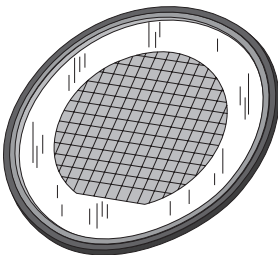
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

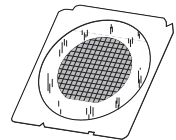
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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