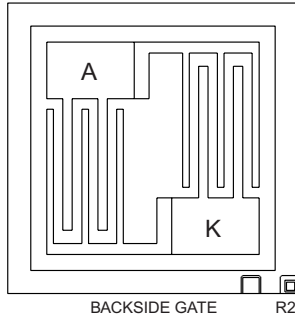


CP622-2N6027

Programmable Unijunction Transistor Die

The CP622-2N6027 is a silicon PUT designed for adjustable characteristics such as Valley Current (I_V), and Peak Current (I_P).



MECHANICAL SPECIFICATIONS:

Die Size	27.5 x 27.5 MILS
Die Thickness	9.45 MILS
Anode Bonding Pad Size	7.1 x 5.1 MILS
Cathode Bonding Pad Size	7.1 x 5.1 MILS
Top Side Metalization	Al – 20,000Å
Back Side Metalization	Au – 13,000Å
Scribe Alley Width	3.6 MILS
Wafer Diameter	3 INCHES
Gross Die Per Wafer	8,894

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

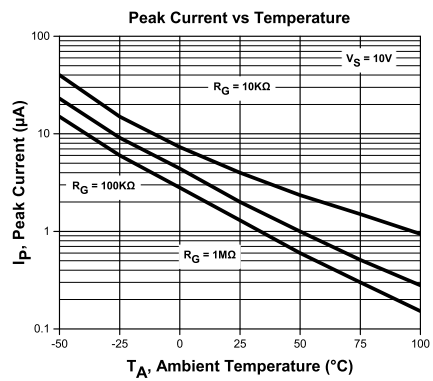
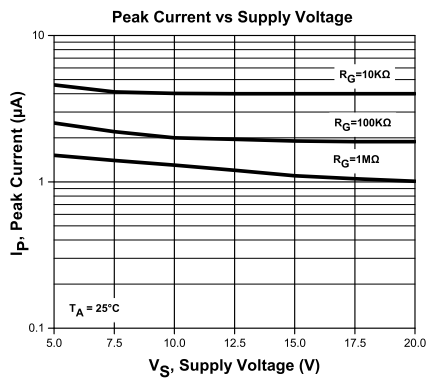
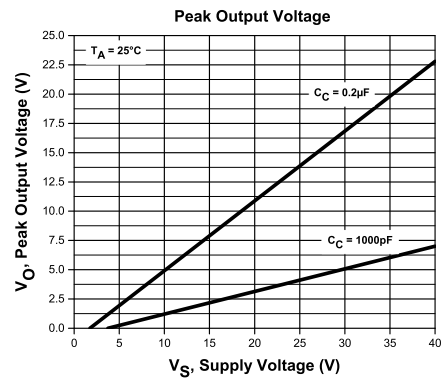
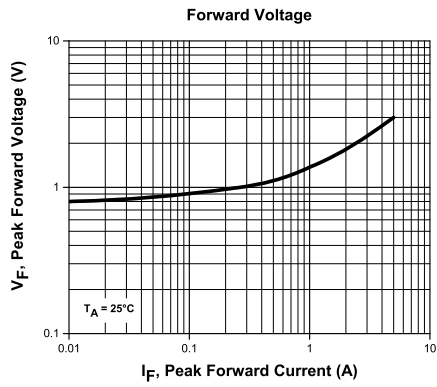
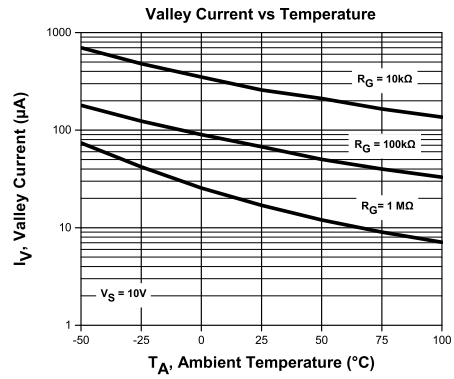
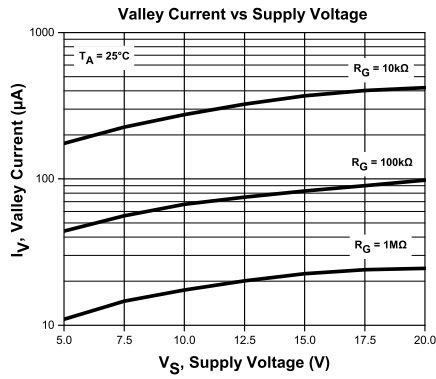
	SYMBOL		UNITS
Gate-Cathode Forward Voltage	V_{GKF}	40	V
Gate-Cathode Reverse Voltage	V_{GKR}	5.0	V
Gate-Anode Reverse Voltage	V_{GAR}	40	V
Anode-Cathode Voltage	V_{AK}	40	V
Peak Non-Repetitive Forward Current ($t=10\mu\text{s}$)	I_{TSM}	5.0	A
Peak Repetitive Forward Current ($t=20\mu\text{s}$, D.C.=1.0%)	I_{TRM}	2.0	A
Peak Repetitive Forward Current ($t=100\mu\text{s}$, D.C.=1.0%)	I_{TRM}	1.0	A
DC Forward Anode Current	I_T	150	mA
DC Gate Current	I_G	50	mA
Operating Junction Temperature	T_J	-50 to +100	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GAO}	$V_S=40\text{V}$		10	nA
I_{GKS}	$V_S=40\text{V}$		50	nA
I_P	$V_S=10\text{V}$, $R_G=1.0\text{M}\Omega$		2.0	μA
I_P	$V_S=10\text{V}$, $R_G=10\text{k}\Omega$		5.0	μA
I_V	$V_S=10\text{V}$, $R_G=1.0\text{M}\Omega$		50	μA
I_V	$V_S=10\text{V}$, $R_G=10\text{k}\Omega$	70		μA
I_V	$V_S=10\text{V}$, $R_G=200\Omega$	1.5		mA
V_T	$V_S=10\text{V}$, $R_G=1.0\text{M}\Omega$	0.2	1.6	V
V_T	$V_S=10\text{V}$, $R_G=10\text{k}\Omega$	0.2	0.6	V
V_F	$I_F=50\text{mA}$		1.5	V
V_O	$V_B=20\text{V}$, $C_C=0.2\mu\text{F}$	6.0		V
t_r	$V_B=20\text{V}$, $C_C=0.2\mu\text{F}$		80	ns

CP622-2N6027

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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