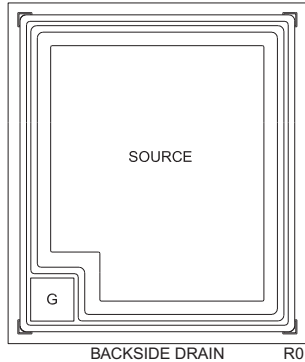


CP726X-CMLDM8120

P-Channel MOSFET Die

Enhancement-Mode

The CP726X-CMLDM8120 is a silicon P-Channel MOSFET designed for power management and load switching applications.



MECHANICAL SPECIFICATIONS:

Die Size	27.6 x 31.5 MILS
Die Thickness	5.5 MILS
Gate Bonding Pad Size	3.9 x 3.9 MILS
Source Bonding Pad Size	20.2 x 24.1 MILS
Top Side Metalization	Al-Si – 35,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	1.97 MILS
Wafer Diameter	6 INCHES
Gross Die Per Wafer	27,100

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL		UNITS
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	8.0	V
Continuous Drain Current (Steady State)	I _D	860	mA
Continuous Drain Current, t≤5.0s	I _D	950	mA
Continuous Source Current (Body Diode)	I _S	360	mA
Maximum Pulsed Drain Current, tp=10μs	I _{DM}	4.0	A
Maximum Pulsed Source Current, tp=10μs	I _{SM}	4.0	A
Operating and Storage Junction Temperature	T _J , T _{stg}	-65 to +150	°C

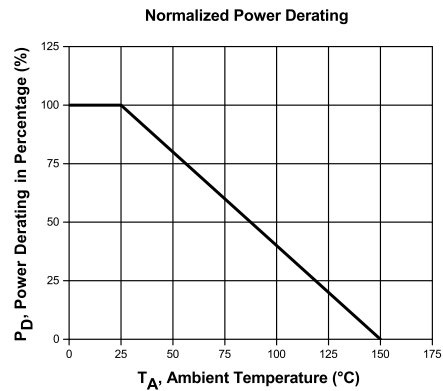
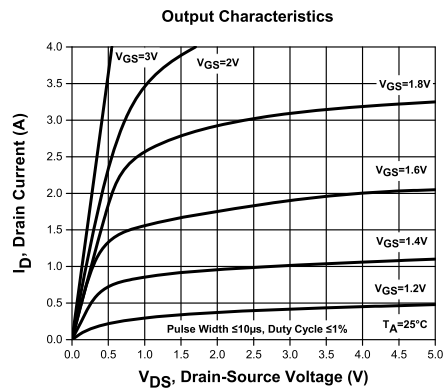
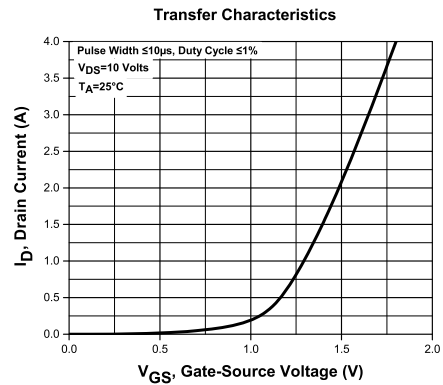
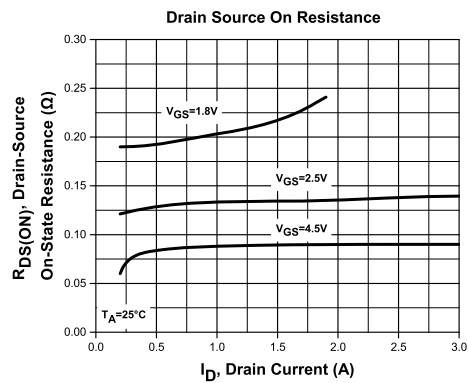
ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I _{GSSS} , I _{GSSR}	V _{GS} =8.0V, V _{DS} =0			50	nA
I _{DSS}	V _{DS} =20V, V _{GS} =0			500	nA
BV _{DSS}	V _{GS} =0, I _D =250μA	20			V
V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45		1.0	V
V _{SD}	V _{GS} =0V, I _S =360mA			0.9	V
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.95A			0.15	Ω
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.77A			0.142	Ω
r _{DS(ON)}	V _{GS} =2.5V, I _D =0.67A			0.20	Ω
r _{DS(ON)}	V _{GS} =1.8V, I _D =0.2A			0.24	Ω
g _{FS}	V _{DS} =10V, I _D =0.81A	2.0			S
C _{rss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		80		pF
C _{iss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		200		pF
C _{oss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		60		pF
Q _{g(tot)}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		3.56		nC
Q _{gs}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		0.36		nC
Q _{gd}	V _{DS} =10V, V _{GS} =4.5V, I _D =1.0A		1.52		nC
t _{on}	[V _{DD} =10V, V _{GS} =4.5V, I _D =0.95A, R _G =6Ω]		20		ns
t _{off}	[V _{DD} =10V, V _{GS} =4.5V, I _D =0.95A, R _G =6Ω]		25		ns

R0 (2-August 2016)

CP726X-CMLDM8120

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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