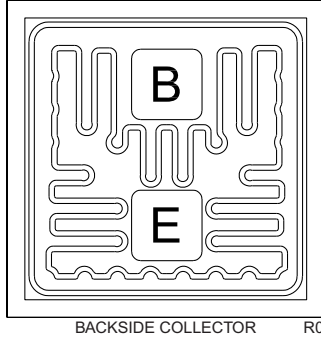


CP741V-CMPT7410

PNP - Low $V_{CE(SAT)}$ Transistor Die

1.0 Amp, 25 Volt

The CP741V-CMPT7410 die is a low $V_{CE(SAT)}$ silicon PNP transistor designed for high current applications.



MECHANICAL SPECIFICATIONS:

Die Size	17.7 x 17.7 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Size	3.8 x 3.8 MILS
Emitter Bonding Pad Size	3.8 x 3.8 MILS
Top Side Metalization	Al-Si – 30,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	1.97 MILS
Wafer Diameter	5 INCHES
Gross Die Per Wafer	54,330

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	40	V
Collector-Emitter Voltage	V_{CEO}	25	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Continuous Collector Current	I_C	1.0	A
Peak Collector Current	I_{CM}	1.5	A
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

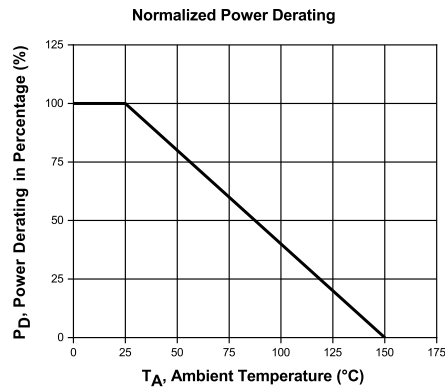
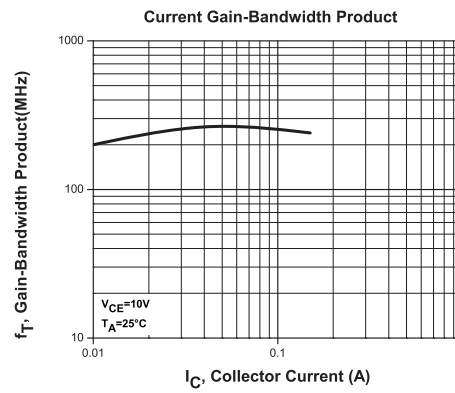
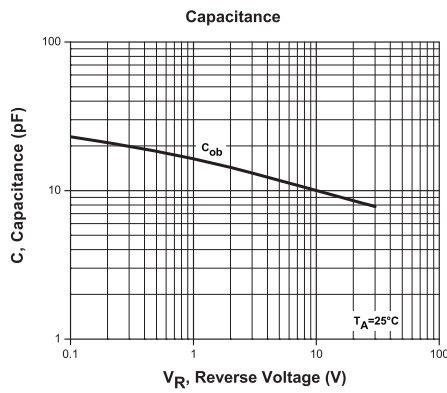
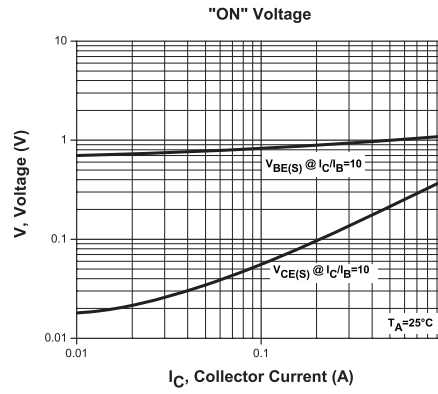
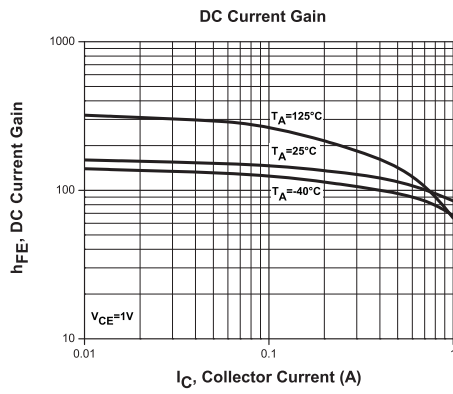
ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=40\text{V}$		100	nA
I_{EBO}	$V_{EB}=6.0\text{V}$		100	nA
BV_{CBO}	$I_C=100\mu\text{A}$	40		V
BV_{CEO}	$I_C=10\text{mA}$	25		V
BV_{EBO}	$I_E=100\mu\text{A}$	6.0		V
$V_{CE(SAT)}$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		50	mV
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=10\text{mA}$		75	mV
$V_{CE(SAT)}$	$I_C=200\text{mA}, I_B=20\text{mA}$		150	mV
$V_{CE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$		250	mV
$V_{CE(SAT)}$	$I_C=800\text{mA}, I_B=80\text{mA}$		400	mV
$V_{CE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		450	mV
$V_{BE(SAT)}$	$I_C=800\text{mA}, I_B=80\text{mA}$		1.1	V
$V_{BE(ON)}$	$V_{CE}=1.0\text{V}, I_C=10\text{mA}$		0.9	V
h_{FE}	$V_{CE}=1.0\text{V}, I_C=10\text{mA}$	100		
h_{FE}	$V_{CE}=1.0\text{V}, I_C=100\text{mA}$	100	300	
h_{FE}	$V_{CE}=1.0\text{V}, I_C=500\text{mA}$	100		
h_{FE}	$V_{CE}=1.0\text{V}, I_C=1.0\text{A}$	50		
f_T	$V_{CE}=10\text{V}, I_C=50\text{mA}, f=100\text{MHz}$	100		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=1.0\text{MHz}$		15	pF

R0 (28-August 2018)

CP741V-CMPT7410

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

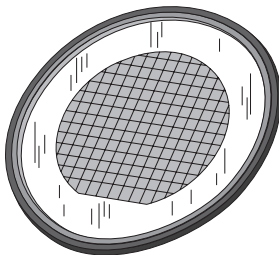
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

Worldwide Distributors:
www.centrasemi.com/wwdistributors

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