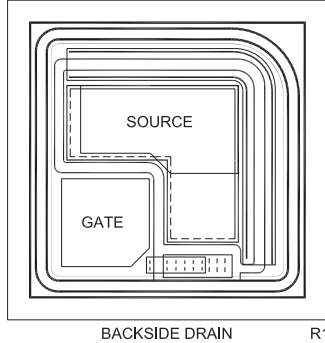


CP761R-CEDM8001

P-Channel MOSFET Die Enhancement-Mode

The CP761R-CEDM8001 is a silicon P-Channel enhancement-mode MOSFET die process designed for high speed pulsed amplifier and driver applications.



MECHANICAL SPECIFICATIONS:

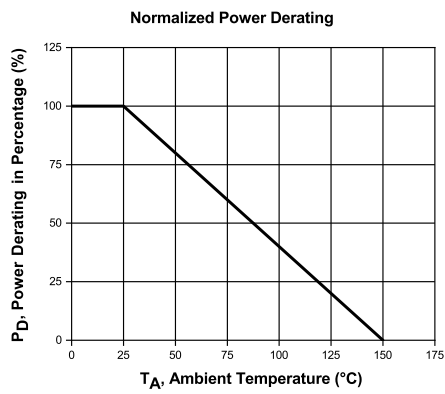
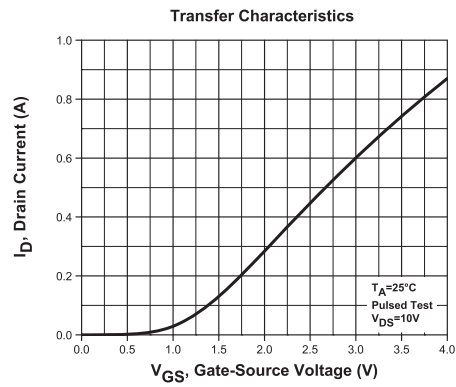
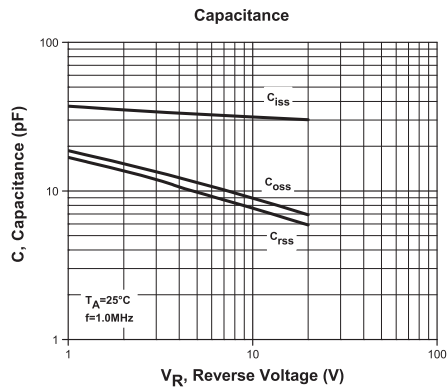
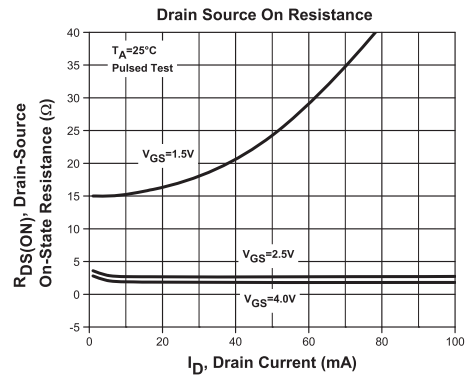
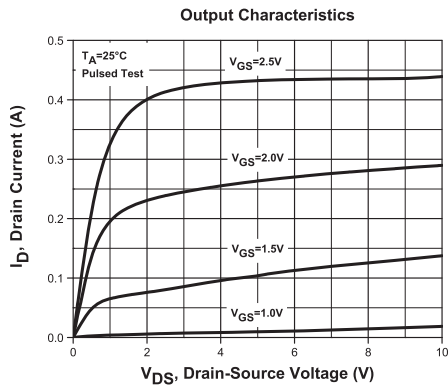
Die Size	14.2 x 14.2 MILS
Die Thickness	3.9 MILS
Gate Bonding Pad Size	3.94 x 3.94 MILS
Source Bonding Pad Size	3.94 x 7.08 MILS
Top Side Metalization	Al-Si – 35,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	2.0 MILS
Wafer Diameter	6 INCHES
Gross Die Per Wafer	123,000

MAXIMUM RATINGS: (T _A =25°C)	SYMBOL		UNITS
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	10	V
Continuous Drain Current (Steady State)	I _D	100	mA
Continuous Drain Current	I _D	200	mA
Operating and Storage Junction Temperature	T _J , T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS: (T _A =25°C unless otherwise noted)						
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
I _{GSSF} , I _{GSSR}	V _{GS} =10V, V _{DS} =0			1.0	µA	
I _{DSS}	V _{DS} =20V, V _{GS} =0			1.0	µA	
BV _{DSS}	V _{GS} =0, I _D =100µA	20			V	
V _{GS(th)}	V _{DS} =V _{GS} , I _D =250µA	0.6		1.1	V	
r _{DS(ON)}	V _{GS} =4.0V, I _D =10mA			8.0	Ω	
r _{DS(ON)}	V _{GS} =2.5V, I _D =10mA			12	Ω	
r _{DS(ON)}	V _{GS} =1.5V, I _D =1.0mA			45	Ω	
g _{FS}	V _{DS} =10V, I _D =100mA	100			mS	
C _{rss}	V _{DS} =3.0V, V _{GS} =0, f=1.0MHz		15		pF	
C _{iss}	V _{DS} =3.0V, V _{GS} =0, f=1.0MHz		45		pF	
C _{oss}	V _{DS} =3.0V, V _{GS} =0, f=1.0MHz		15		pF	
Q _{g(tot)}	V _{DS} =10V, V _{GS} =4.5V, I _D =100mA		0.658		nC	
Q _{gs}	V _{DS} =10V, V _{GS} =4.5V, I _D =100mA		0.158		nC	
Q _{gd}	V _{DS} =10V, V _{GS} =4.5V, I _D =100mA		0.181		nC	
t _{on}	V _{DD} =3.0V, V _{GS} =2.5V, I _D =10mA		35		ns	
t _{off}	V _{DD} =3.0V, V _{GS} =2.5V, I _D =10mA		80		ns	

CP761R-CEDM8001

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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