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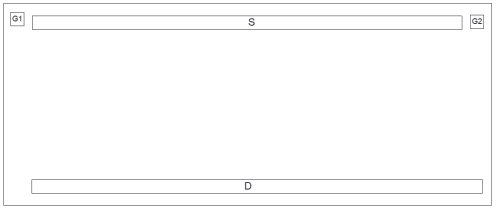
CPG003-CDFG6511N

650V Gallium Nitride Enhancement-Mode Power FET

The CPG003-CDFG6511N is a 650V GaN on silicon Enhancement mode power FET designed for low gate charge, low output charge and ultra high switching frequency applications.



BACKSIDE NO CONNECTION R0

MECHANICAL SPECIFICATIONS:

Die Size	132 x 55 MILS
Die Thickness	45.2 MILS
Gate Bonding Pad Size	3.54 x 3.54 MILS
Drain Bonding Pad Size	119.4 x 3.54 MILS
Source Bonding Pad Size	113.4 x 3.54 MILS
Top Side Metalization	Al-Cu – 35,000Å
Back Side Metalization	Si – 21,000Å
Scribe Alley Width	3.15 MILS
Wafer Diameter	8 INCHES
Gross Die Per Wafer	5,719

MAXIMUM RATINGS: (T_J=25°C)	**SYMBOL**		**UNITS**
Continuous Drain-Source Voltage	V_{DS}	650	V
Transient Drain-Source Voltage (tp<200µs)	V_{DS}	800	V
Pulsed Drain-Source Voltage (tp<100ns)	V_{DS}	750	V
Continuous Gate-Source Voltage	V_{GS}	-1.4 to +7	V
Pulsed Gate-Source Voltage (tp=50ns)	V_{GS}	-20 to +10	V
Continuous Drain Current (T_C=25°C)	I_D	11.5	A
Pulsed Drain Current (T_C=25°C, tp=10µs)	I_{DM}	20.5	A
Pulsed Drain Current (T_C=125°C, tp=10µs)	I_{DM}	11.5	A
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	°C

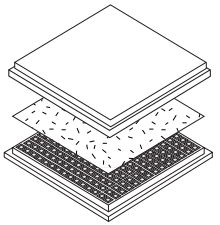
ELECTRICAL CHARACTERISTICS: (T_J=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}	V_{GS}=6V, V_{DS}=0		60		µA
I_{DSS}	V_{DS}=650V, V_{GS}=0		0.45	20	µA
I_{DSS}	V_{DS}=650V, V_{GS}=0, T_J=150°C		6.0		µA
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=12.2mA	1.2	1.7	2.5	V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=12.2mA, T_J=150°C		1.7		V
V_{SD}	V_{GS}=0, I_S=3.9A		2.6		V
$r_{DS(ON)}$	V_{GS}=6.0V, I_D=3.9A		138	190	mΩ
$r_{DS(ON)}$	V_{GS}=6.0V, I_D=3.9A, T_J=150°C		300		mΩ
R_{G1}	f=5.0MHz		5		Ω
R_{G2}	f=5.0MHz		6		Ω
C_{iss}	V_{DS}=400V, V_{GS}=0, f=100kHz		96		pF
C_{oss}	V_{DS}=400V, V_{GS}=0, f=100kHz		30		pF
C_{rss}	V_{DS}=400V, V_{GS}=0, f=100kHz		0.5		pF

ELECTRICAL CHARACTERISTICS: (T_J=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$C_{o(er)}$	V_{DS}=0 to 400V, V_{GS}=0		43		pF
$C_{o(tr)}$	V_{DS}=0 to 400V, V_{GS}=0		60		pF
Q_{oss}	V_{DS}=0 to 400V, V_{GS}=0		24.5		nC
$t_{d(on)}$	V_{DS}=400V, V_{GS}=6V, I_D=8A, L=318µH, R_{on}=10Ω, R_{off}=2Ω		1.4		ns
$t_{d(off)}$	V_{DS}=400V, V_{GS}=6V, I_D=8A, L=318µH, R_{on}=10Ω, R_{off}=2Ω		1.7		ns
t_r	V_{DS}=400V, V_{GS}=6V, I_D=8A, L=318µH, R_{on}=10Ω, R_{off}=2Ω		4.0		ns
t_f	V_{DS}=400V, V_{GS}=6V, I_D=8A, L=318µH, R_{on}=10Ω, R_{off}=2Ω		4.0		ns
$Q_{g(tot)}$	V_{DS}=400V, V_{GS}=0 to 6V, I_D=3.9A		2.8		nC
Q_{gs}	V_{DS}=400V, V_{GS}=0 to 6V, I_D=3.9A		0.25		nC
Q_{gd}	V_{DS}=400V, V_{GS}=0 to 6V, I_D=3.9A		1.1		nC
Q_{rr}	I_D=3.9A, V_{DS}=400V		0		nC
t_{rr}			0		ns

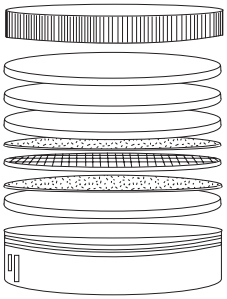
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

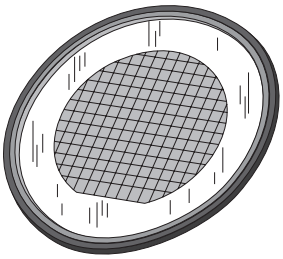
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



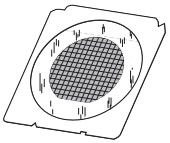
UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)



Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.

Visit the Central website for a complete listing of specifications:
www.centralsemi.com/bdspecs

R2 (3-April 2017)

OUTSTANDING SUPPORT AND SUPERIOR SERVICES

PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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