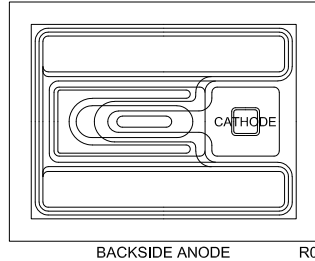


CPZ52R-CFTVS5V0BULC

Low Capacitance TVS Die

5.0 Volt

The CPZ52R-CFTVS5V0BULC is a silicon, low capacitance transient voltage suppressor designed to protect sensitive equipment connected to high speed data lines against ESD damage. In order to accomplish bi-directional functionality, two CPZ52R-CFTVS5V0BULC die must be configured back-to-back (Cathode-to-Cathode).



MECHANICAL SPECIFICATIONS:

Die Size	14.2 x 11 MILS
Die Thickness	3.9 MILS
Cathode Bonding Pad Size	3.15 x 3.15 MILS
Top Side Metalization	Al-Si – 30,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	1.97 MILS
Wafer Diameter	6 INCHES
Gross Die Per Wafer	136,207

MAXIMUM RATINGS: (T_A=25°C)

	SYMBOL		UNITS
Peak Power Dissipation (8x20μs)	P _{PK}	14	W
Electrical Fast Transient (IEC 61000-4-4) (5x50ns)	EFT	40	A
ESD Voltage (IEC 61000-4-2, Air)	V _{ESD}	20	kV
ESD Voltage (IEC 61000-4-2, Contact)	V _{ESD}	20	kV
Operating Junction Temperature	T _J	-55 to +125	°C
Storage Temperature	T _{stg}	-55 to +150	°C

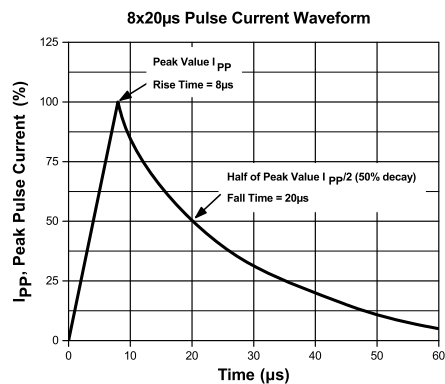
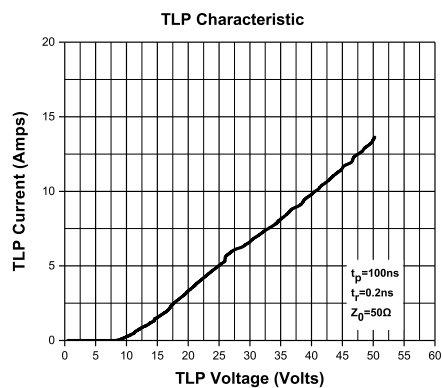
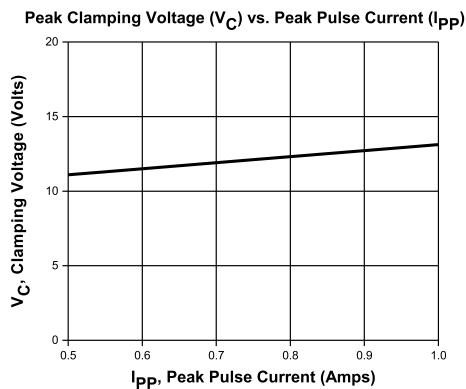
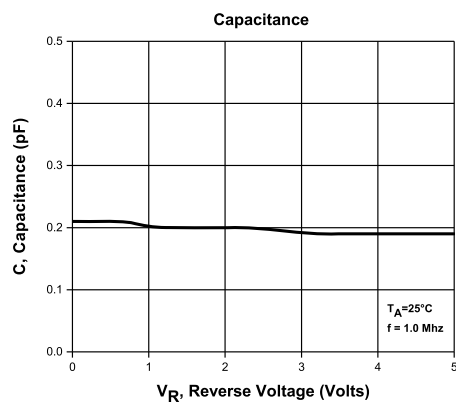
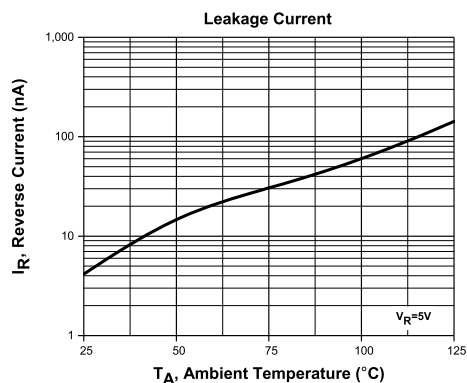
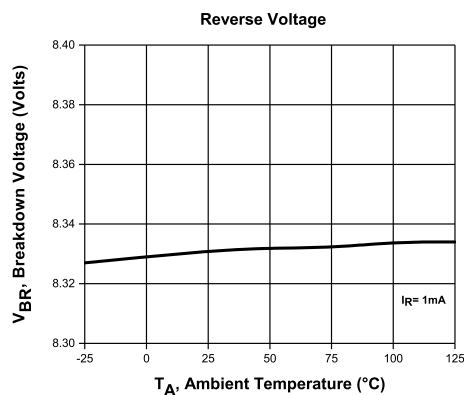
ELECTRICAL CHARACTERISTICS PER BACK-TO-BACK TVS PAIR: (T_A=25°C)

Maximum Reverse Stand-off Voltage	Breakdown Voltage		Test Current	Maximum Reverse Leakage Current	Maximum Clamping Voltage (8x20μs)		Typical TLP Clamping Voltage (Note 1)		Typical Dynamic Resistance (Note 1)	Typical Junction Capacitance @ 0V Bias	Maximum Junction Capacitance @ 0V Bias
V _{RWM}	V _{BR} @ I _T		I _T	I _R @ V _{RWM}	V _C @ I _{PP}		V _{CL} @ I _{PP}		R _{DYN}	C _J	C _J
V	MIN V	MAX V	mA	nA	V	A	V	A	Ω	pF	pF
5.0	6.0	10	1.0	100	14	1.0	15	1.6	2.94	0.2	0.35
							20	3.3			

Note 1: Transmission Line Pulse (TLP) conditions: Z₀=50Ω, t_p=100ns

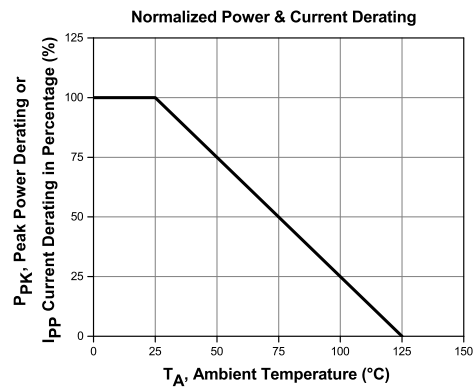
CPZ52R-CFTVS5V0BULC

Typical Electrical Characteristics

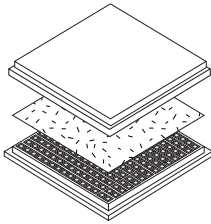


CPZ52R-CFTVS5V0BULC

Typical Electrical Characteristics



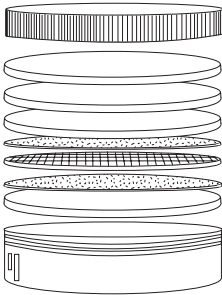
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

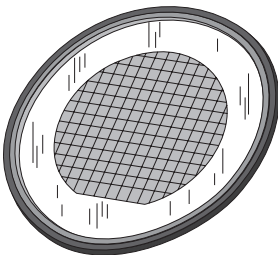
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

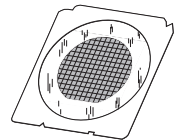
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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