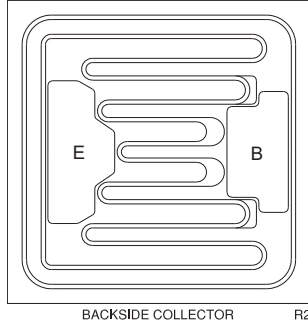


The CP305-2N3019 is a silicon NPN transistor designed for high current, general purpose applications.



MECHANICAL SPECIFICATIONS:

Die Size	31 x 31 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Size	5.9 x 11.8 MILS
Emitter Bonding Pad Size	6.5 x 13.8 MILS
Top Side Metalization	Al – 30,000Å
Back Side Metalization	Au – 18,000Å
Scribe Alley Width	1.96 MILS
Wafer Diameter	4 INCHES
Gross Die Per Wafer	11,212

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	140	V
Collector-Emitter Voltage	V_{CEO}	80	V
Emitter-Base Voltage	V_{EBO}	7.0	V
Continuous Collector Current	I_C	1.0	A
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$)

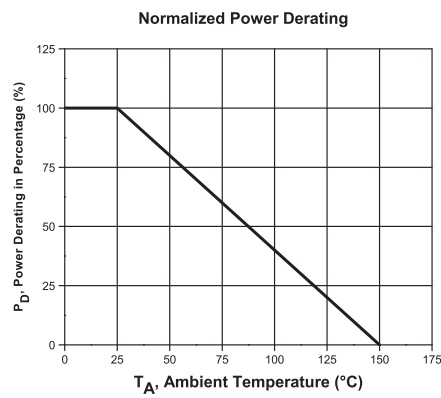
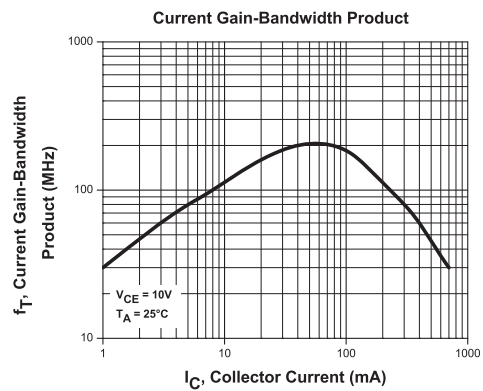
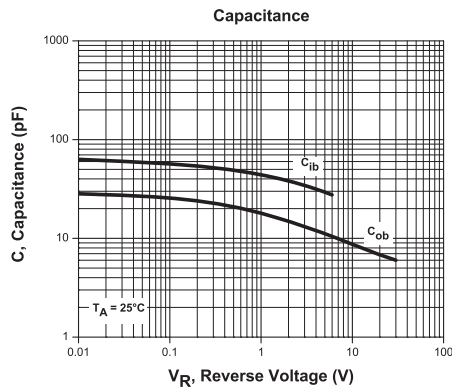
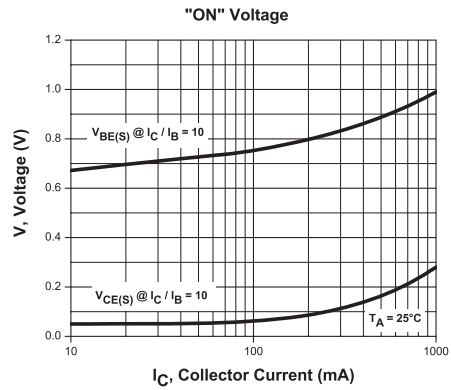
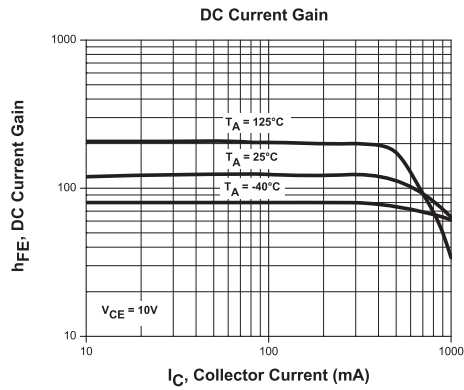
SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=90\text{V}$		10	nA
I_{EBO}	$V_{EB}=5.0\text{V}$		10	nA
BV_{CBO}	$I_C=100\mu\text{A}$	140		V
BV_{CEO}	$I_C=30\text{mA}$	80		V
BV_{EBO}	$I_E=100\mu\text{A}$	7.0		V
$V_{CE(SAT)}$	$I_C=150\text{mA}, I_B=15\text{mA}$		0.2	V
$V_{CE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$		0.5	V
$V_{BE(SAT)}$	$I_C=150\text{mA}, I_B=15\text{mA}$		1.1	V
h_{FE}	$V_{CE}=10\text{V}, I_C=100\mu\text{A}$	50		
h_{FE}	$V_{CE}=10\text{V}, I_C=10\text{mA}$	90		
h_{FE}	$V_{CE}=10\text{V}, I_C=150\text{mA}$	100	300	
h_{FE}	$V_{CE}=10\text{V}, I_C=500\text{mA}$	50		
h_{FE}	$V_{CE}=10\text{V}, I_C=1.0\text{A}$	15		
f_T	$V_{CE}=10\text{V}, I_C=50\text{mA}, f=20\text{MHz}$	100		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=1.0\text{MHz}$		12	pF
C_{ib}	$V_{EB}=0.5\text{V}, I_C=0, f=1.0\text{MHz}$		60	pF

PACKING OPTIONS:

- CP305-2N3019-CT: Singulated die in waffle pack; 400 die per tray.
- CP305-2N3019-WN: Full wafer, unsawn, 100% tested with reject die inked.
- CP305-2N3019-WR: Full wafer, sawn and mounted on plastic ring, 100% tested with reject die inked.

CP305-2N3019

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

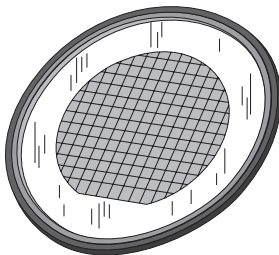
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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