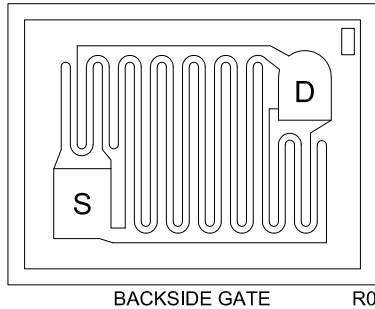


The CP216-2N4392 is a silicon N-Channel small signal JFET designed for analog switching and chopper applications.



MECHANICAL SPECIFICATIONS:

| | |
|-------------------------|----------------|
| Die Size | 21 x 16 MILS |
| Die Thickness | 7.9 MILS |
| Drain Bonding Pad Size | 3.3 x 4.5 MILS |
| Source Bonding Pad Size | 3.3 x 4.5 MILS |
| Top Side Metalization | Al – 10,000Å |
| Back Side Metalization | Au – 3,250Å |
| Scribe Alley Width | 2.0 MILS |
| Wafer Diameter | 4 INCHES |
| Gross Die Per Wafer | 29,732 |

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

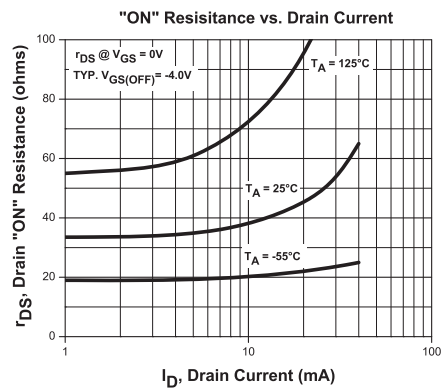
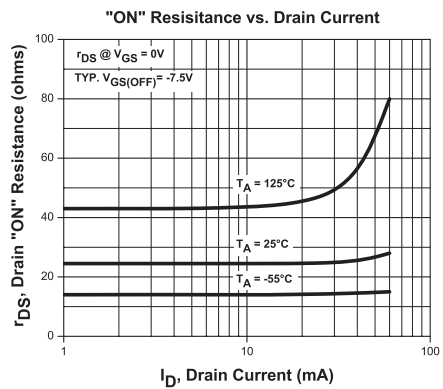
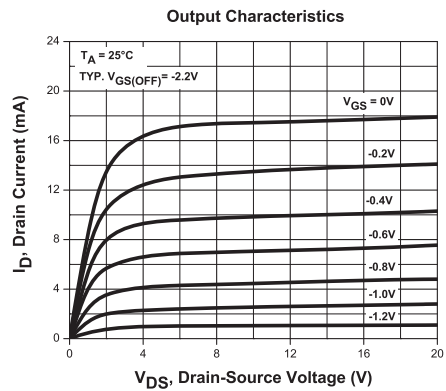
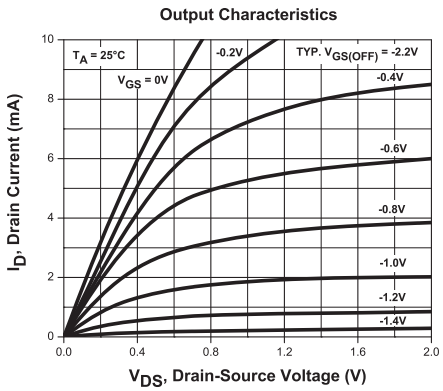
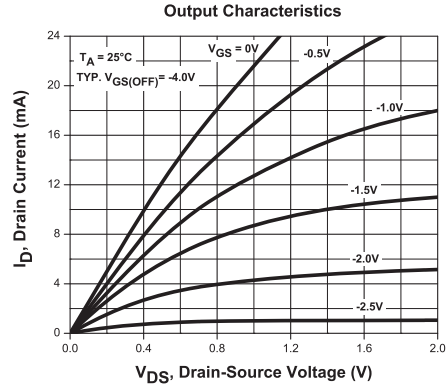
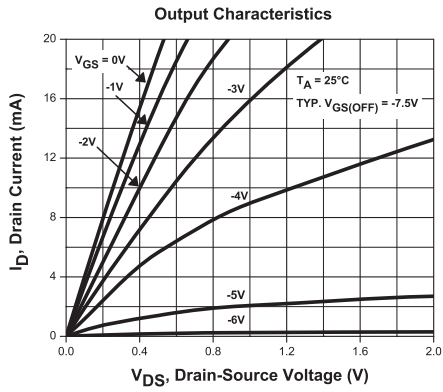
| | SYMBOL | | UNITS |
|--|----------------|-------------|------------------|
| Gate-Drain Voltage | V_{GD} | 40 | V |
| Gate-Source Voltage | V_{GS} | 40 | V |
| Gate Current | I_G | 50 | mA |
| Operating and Storage Junction Temperature | T_J, T_{stg} | -65 to +175 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

| SYMBOL | TEST CONDITIONS | MIN | MAX | UNITS |
|---------------|-----------------------------------|-----|-----|----------|
| I_{GSS} | $V_{GS}=20V$ | | 0.1 | nA |
| I_{DSS} | $V_{DS}=20V$ | 25 | 75 | mA |
| $I_{D(OFF)}$ | $V_{DS}=20V, V_{GS}=7.0V$ | | 0.1 | nA |
| BV_{GSS} | $I_G=1.0\mu A$ | 40 | | V |
| $V_{GS(OFF)}$ | $V_{DS}=20V, I_D=1.0nA$ | 2.0 | 5.0 | V |
| $V_{GS(f)}$ | $V_{DS}=0, I_G=1.0mA$ | | 1.0 | V |
| $V_{DS(ON)}$ | $I_D=6.0mA$ | | 0.4 | V |
| $r_{DS(ON)}$ | $I_D=1.0mA, V_{GS}=0$ | | 60 | Ω |
| C_{rss} | $V_{GS}=7.0V, V_{DS}=0, f=1.0MHz$ | | 3.5 | pF |
| C_{iss} | $V_{DS}=20V, V_{GS}=0, f=1.0MHz$ | | 14 | pF |
| t_{on} | $I_{D(ON)}=6.0mA$ | | 15 | ns |
| t_{off} | $V_{GS(OFF)}=7.0V$ | | 35 | ns |

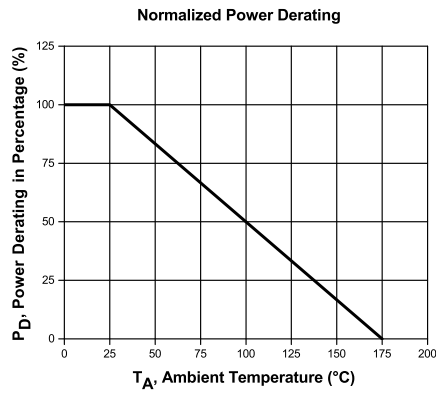
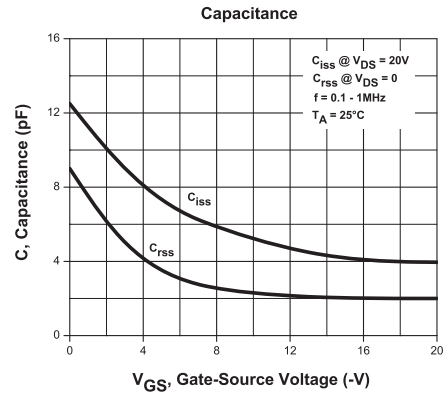
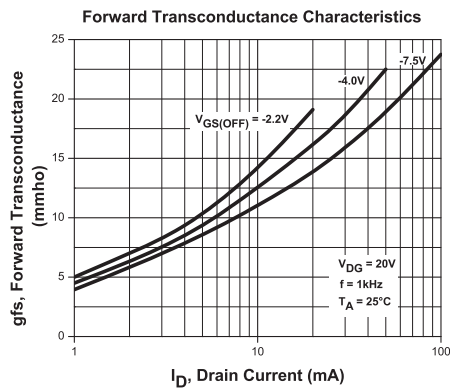
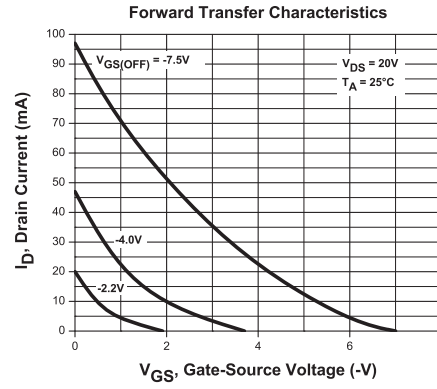
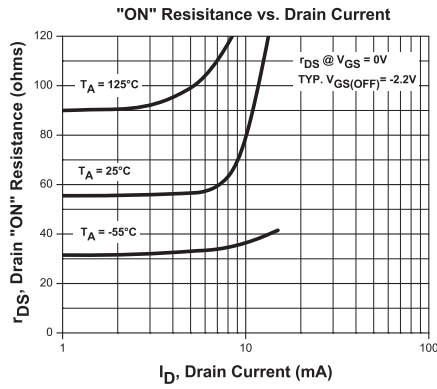
CP216-2N4392

Typical Electrical Characteristics



CP216-2N4392

Typical Electrical Characteristics



R1 (23-May 2018)

BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

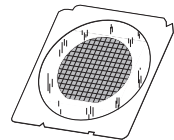
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

Worldwide Distributors:
www.centrasemi.com/wwdistributors

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