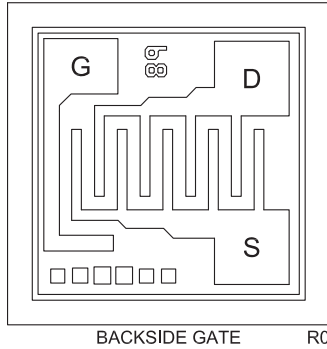


The CP654-2N5460 is a silicon P-Channel JFET designed for low level amplifier applications.



MECHANICAL SPECIFICATIONS:

Die Size	20 x 20 MILS
Die Thickness	8.0 MILS
Gate Bonding Pad Size	3.0 x 4.0 MILS
Drain Bonding Pad Size	4.0 x 4.0 MILS
Source Bonding Pad Size	4.0 x 4.0 MILS
Top Side Metalization	Al – 30,000Å
Back Side Metalization	Au – 6,000Å
Scribe Alley Width	1.0 MILS
Wafer Diameter	4 INCHES
Gross Die Per Wafer	20,213

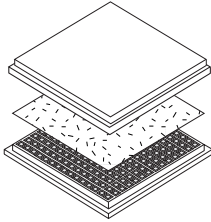
MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

	SYMBOL		UNITS
Drain-Gate Voltage	V_{DG}	40	V
Reverse Gate-Source Voltage	V_{GSR}	40	V
Continuous Gate Current	I_G	10	mA
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSS}	$V_{GS}=20\text{V}, V_{DS}=0$		5.0	nA
I_{DSS}	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{kHz}$	1.0	5.0	mA
BV_{GSS}	$I_G=10\mu\text{A}$	40		V
V_{GS}	$V_{DS}=15\text{V}, I_D=0.1\text{mA}$	0.5	4.0	V
$V_{GS(OFF)}$	$V_{DS}=15\text{V}, I_D=1.0\mu\text{A}$	0.75	6.0	V
$ y_{fs} $	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{kHz}$	1.0K	4.0K	μS
$ y_{os} $	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{kHz}$		75	μS
C_{rss}	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$		2.0	pF
C_{iss}	$V_{DS}=15\text{V}, V_{GS}=0, f=1.0\text{MHz}$		7.0	pF
e_N	$V_{DS}=15\text{V}, V_{GS}=0, f=100\text{Hz}, \text{BW}=1.0\text{Hz}$		115	$\text{nV}/\sqrt{\text{Hz}}$
NF	$V_{DS}=15\text{V}, V_{GS}=0, f=100\text{Hz}, R_G=1.0\text{M}\Omega, \text{BW}=1.0\text{Hz}$		2.5	dB

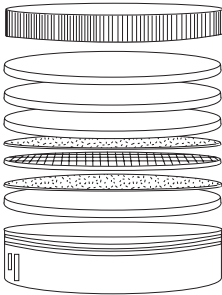
BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

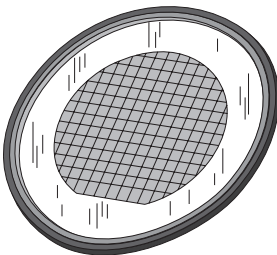
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

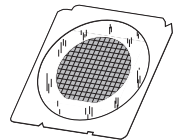
WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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