

**CMNTVS12V**  
**SURFACE MOUNT SILICON**  
**UNI-DIRECTIONAL**  
**12 VOLT QUAD TVS ARRAY**



[www.centrasemi.com](http://www.centrasemi.com)

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMNTVS12V is a 4-line TVS arrays in a space saving SOT-953 surface mount package. This device is designed to protect sensitive equipment against ESD damage.

**MARKING CODE: CY**



**SOT-953 CASE**

- Device is *Halogen Free* by design

**APPLICATIONS:**

- PDAs
- Memory Card Ports
- Mobile Phones
- Instrumentation

**FEATURES:**

- Small, 1.0 x 0.8mm, SOT-953 Surface Mount Package
- Low Capacitance
- Low Leakage Current
- 4-Line Array

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Peak Power Dissipation (8x20 $\mu\text{s}$ )  
 Electrical Fast Transient (IEC 61000-4-4) (5x50ns)  
 ESD Voltage (IEC 61000-4-2, Air)  
 ESD Voltage (IEC 61000-4-2, Contact)  
 Operating and Storage Junction Temperature

**SYMBOL**

$P_{PK}$  18  
 EFT 40  
 $V_{ESD}$  8.0  
 $V_{ESD}$  8.0  
 $T_J, T_{stg}$  -55 to +150

**UNITS**

W  
 A  
 kV  
 kV  
 $^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS PER DIODE:** ( $T_A=25^\circ\text{C}$ )

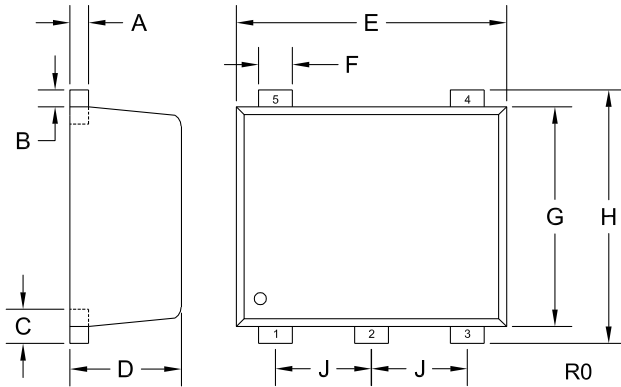
Reverse Breakdown Voltage $V_{BR} @ 5.0\text{mA}$			Maximum Reverse Leakage Current $I_R @ V_{RWM}$		Maximum Clamping Voltage (8x20 $\mu\text{s}$ ) $V_C @ I_{PP}$		Typical TLP Clamping Voltage (Note 1) $V_{CL} @ I_{PP}$		Typical Dynamic Resistance (Note 1) $R_{DYN}$	Maximum Junction Capacitance @ 0V Bias $C_J$	Maximum Junction Capacitance @ 3V Bias $C_J$
MIN V	NOM V	MAX V	$\mu\text{A}$	V	V	A	V	A	$\Omega$	pF	pF
11.4	12.0	12.7	0.5	9.0	18	1.0	20	3.5	2.56	10	6.0
							30	7.4			

Note 1: Transmission Line Pulse (TLP) conditions:  $Z_0=50\Omega$ ,  $t_p=100\text{ns}$

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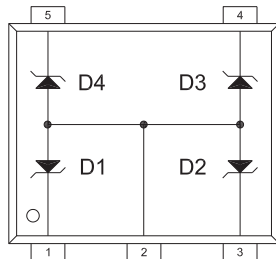
**SOT-953 CASE - MECHANICAL OUTLINE**



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.002	0.006	0.050	0.150
B	0.002	0.006	0.050	0.150
C	0.005	0.007	0.125	0.175
D	0.016	0.020	0.400	0.500
E	0.037	0.041	0.950	1.050
F	0.004	0.008	0.100	0.200
G	0.030	0.033	0.750	0.850
H	0.037	0.041	0.950	1.050
J	0.014		0.350	

SOT-953 (REV: R0)

**PIN CONFIGURATION**



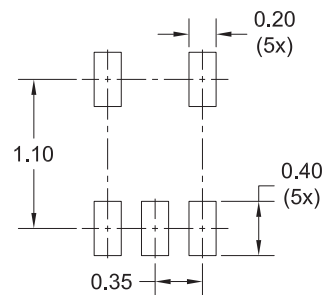
**LEAD CODE:**

- 1) Cathode D1
- 2) Anode D1, D2, D3, D4
- 3) Cathode D2
- 4) Cathode D3
- 5) Cathode D4

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**SUGGESTED MOUNTING PADS**

(Dimensions in mm)



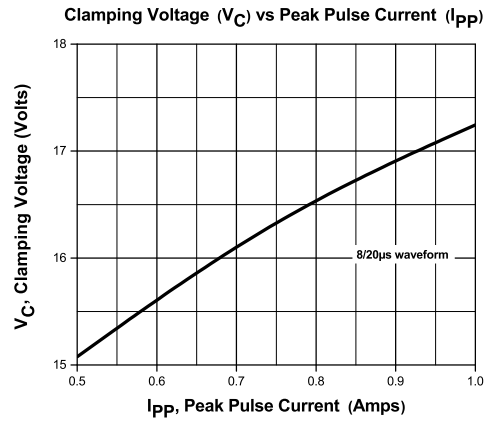
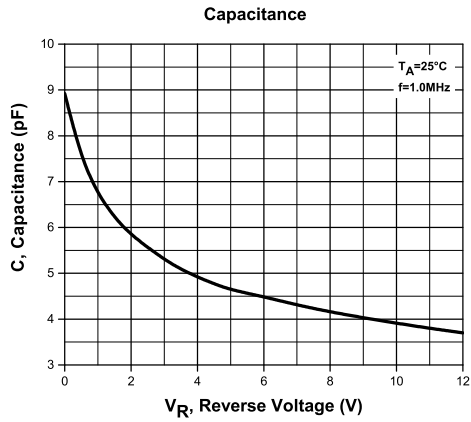
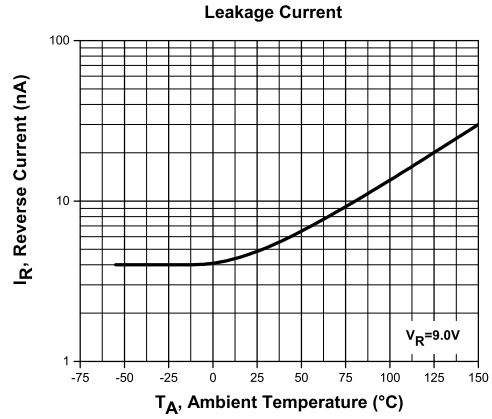
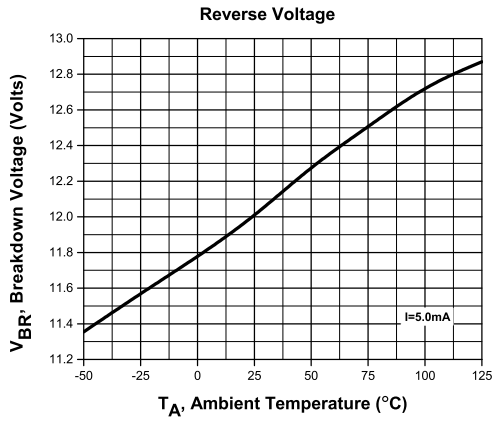
R0

R5 (29-October 2015)

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**TYPICAL ELECTRICAL CHARACTERISTICS**

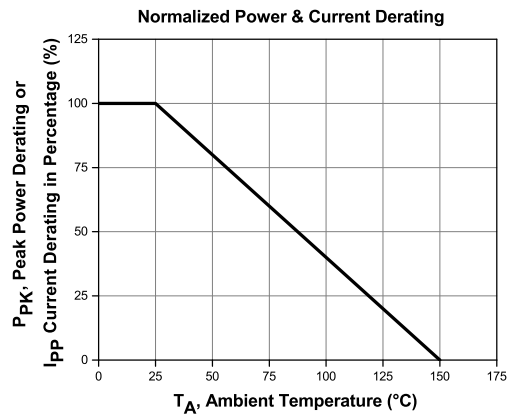
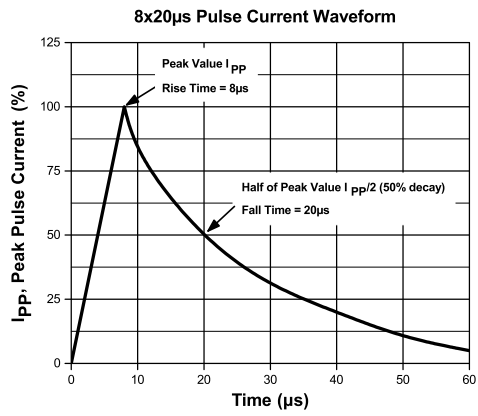
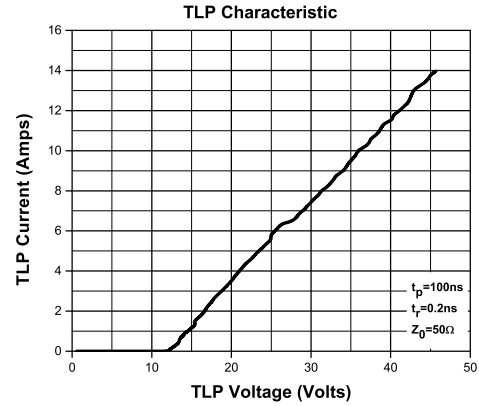
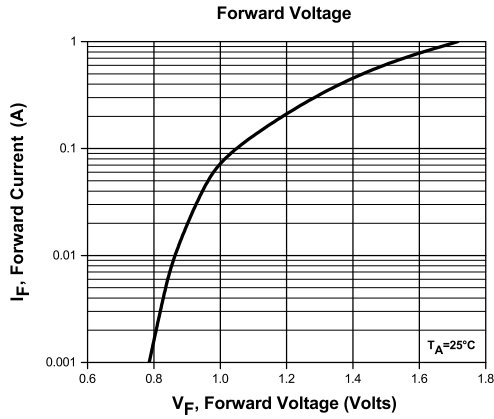


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**TYPICAL ELECTRICAL CHARACTERISTICS**



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## OUTSTANDING SUPPORT AND SUPERIOR SERVICES



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### PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

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### DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2<sup>nd</sup> day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

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### REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

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### CONTACT US

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